Final Report for NASA AISR funded project
Grant number: NNG06GE54G
Project Title: An Integrated Software Environment to Design Polymorphic Fault Tolerant Processors on Radiation Hardened FPGAs
PI: Dr. Aravind Dasu

Milestones accomplished from 2007 to 2009

1. Designed and developed a C to RTL compiler to rapidly compile software code written for simulated annealing based scheduling algorithms onto FPGAs.
2. Benchmarked performance against PowerPC 750 processors with the help of Dr. Steve Chien's group at NASA JPL.
3. Reference code has been uploaded onto EO-1 satellite and awaiting results in October.
4. Designed the first run time re-scalable systolic array accelerator on FPGAs.
5. Demonstrated the design for Extended Kalman filter and 2D Discrete Wavelet Transform.
6. This technology enables real time partial dynamic reconfiguration of any signal processing algorithm on an FPGA.
7. Invited to give a talk on this technology at NASA Ames Research Center on August 4th 2009. Invitation extended by Dr. Zornetzer (NASA ARC).
8. Presented 3 conference papers, published 3 journal papers. All papers have or are being uploaded onto the AISR web repository.
9. Mentored and graduated/graduating 5 students (3 MS and 2 PhD). All have been/are being placed successfully in the high tech industry/national labs.

The thesis and papers authored as a result of the AISR funding have or are being uploaded onto the AISR web repository. They can be accessed at http://aisrp.nasa.gov/